What is claimed is:

1. A semiconductor integrated device provided with a conductive layer and an interlayer insulating film both of which are formed on a semiconductor substrate, the semiconductor integrated device comprising:

a first insulating film formed on any one of the conductive layer and the interlayer insulating film;

a two-layer pad including an upper layer pad and a lower layer pad, the lower layer pad being formed on the first insulating film;

a second insulating film formed on any one of the conductive layer and the interlayer insulating film, the second insulating film having a film thickness greater than that of the first insulating film;

a third insulating film deposited on both of the first insulating film and the lower layer pad of the two-layer pad;

a conductive plug for connecting the upper pad and lower pad of the two-layer pad, the conductive plug being formed in the third insulating film;

the upper layer pad of the two-layer pad being formed on the third insulating film; and

a single-layer pad formed on the second insulating film,

wherein the single-layer pad is bonded without a bonding wire, and the second layer pad of the two-layer pad is bonded with the bonding wire.

2. The semiconductor integrated device, according to claim 1,

wherein the first, second, and third insulating films are

silicon oxide films.

3. The semiconductor integrated device, according to claim 2, wherein a film thickness of each silicon oxide film is approximately 0.5 μm to 1.0 μm.

4. The semiconductor integrated device, according to claim 1, wherein the first, second, and third insulating films are silicon nitride films.

5. The semiconductor integrated device, according to claim 4, wherein a film thickness of each silicon nitride film is approximately 0.5 μm to 1.0 μm.

6. The semiconductor integrated device, according to claim 1, further comprising:

a circuit pattern under both of the single-layer pad and the two-layer pad.

7. The semiconductor integrated device, according to claim 6, wherein the circuit pattern is an I/O buffer.

8. The semiconductor integrated device, according to claim 1, wherein the two-layer pad is arranged against a chip edge of the semiconductor integrated device, and the single-layer pad is arranged inside the two-layer pad.

9. The semiconductor integrated device, according to claim 1,

wherein the single-layer pad is arranged against a chip edge of the semiconductor integrated device, and the two-layer pad is arranged inside the single-layer pad.

10. The semiconductor integrated device, according to claim 1,

wherein a first layout configuration is formed in which the single-layer pad is arranged against a chip edge and in which the two-layer pad is arranged inside the single-layer pad, and

wherein, next to the first layout configuration, a second layout configuration is formed in which the two-layer pad is arranged against the chip edge and in which the single-layer pad is arranged inside the two-layer pad, and

wherein the first and second layout configurations are alternately adopted to arrange the two-layer pads and the single-layer pads.

11. A semiconductor device comprising:

a semiconductor chip;

an internal circuit area provided in said semiconductor chip, said internal circuit area including a functional block;

a plurality of buffer areas provided to surround said internal circuit area, each of said buffer areas including an input/output buffer; and

a plurality of pad structures each provided above an associated one of said buffer areas, each of said pad structure including an interlayer insulating layer, a bonding pad formed on said interlayer insulating layer, a test pad formed on said interlayer insulating layer apart from said bonding pad, a

conductive line electrically connecting said bonding pad and test pad with each other, an intermediate pad layer embedded in said interlayer insulating layer, at least one first contact plug selectively formed in a part of said interlayer insulating layer sandwiched between said bonding pad and said intermediate pad layer to thereby form an conductive path therebetween, and a passivation film formed to cover said boding pad and said test pad and having first and second openings that expose respective parts of said bonding pad and said test pad.

12. The device as claimed in claim 11, further comprising an insulating film covering said semiconductor chip, al least one interconnection layer provided between said insulating film and said interlayer insulating layer.

13. The device as claimed in claim 12, wherein said pad structure further includes at least one second conductive plug selectively formed in a part of said interlayer insulating layer between said intermediate pad layer and said interconnection line to thereby form a conductive path therebetween.

14. The device as claimed in claim 13, wherein said second conductive plug is provided apart in plan view from said bonding pad.